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1. A fabrication method of forming a trenched DMOS device and a termination structure thereof, the method comprising:

forming an N- epitaxial layer on an N+ silicon substrate;

forming an oxide layer on the N- epitaxial layer;

patterning the oxide layer to form a termination oxide layer therein to define an exposed active area of the DMOS device;

implanting P-type ions into the active area by using the termination oxide layer as a mask to form a P body in the N- epitaxial layer;

recessing the N- epitaxial layer to form a plurality of DMOS trenches in the P body by patterning and etching, the DMOS trenches having bottoms which extend beneath a bottom of the P body;

forming a gate oxide layer over exposed surfaces of the P body;

depositing a polysilicon layer over exposed surfaces and also filling the DMOS trenches;

recessing the polysilicon layer to form a plurality of polysilicon gates and a polysilicon plate by patterning and etching, wherein the polysilicon gates are positioned in the DMOS trenches and the polysilicon plate is positioned over the termination oxide layer and a portion of the gate oxide layer disposed adjacent the termination oxide layer;

implanting N-type ions into the P body by using the polysilicon plate and the termination oxide layer as a mask to form a plurality of N+ diffused regions;

forming an isolation layer over exposed surfaces after implanting the N-type ions;

patterning and anisotropically etching the isolation layer and the gate oxide layer to form a plurality of body contact windows over the N+ diffused regions, and a first contact window over the polysilicon plate;

implanting P-type ions through the body contact windows to form a plurality of P+ diffused regions; and

forming a source metal contact layer disposed over the isolation layer, and filling the body contact windows and the first contact window.

2. The method of claim 1, wherein the oxide layer on the N- epitaxial layer is formed by thermal oxidation.

3. The method of claim 1, wherein the gate oxide layer is formed over the exposed surfaces of the P body by thermal oxidation.

4. The method of claim 1, further comprising forming a drain metal contact layer on a back surface of the N+ silicon substrate.

5. The method of claim 4, further comprising removing unnecessary layers formed on the back surface of the N+ silicon substrate prior to forming the drain metal contact layer.

6. The method of claim 5, wherein the unnecessary layers formed o the back surface of the N+ silicon substrate are removed by chemical mechanical polishing.

7. The method of claim 1, further comprising forming a sacrificial oxide layer on the active area after forming the termination oxide layer.

8. The method of claim 6, further comprising removing the sacrificial oxide layer by etching after forming the DMOS trenches but before forming the gate oxide layer.

9. The method of claim 1, wherein the polysilicon plate comprises a portion extending toward one of the DMOS trenches disposed closest to the polysilicon plate.

10. The method of claim 1, wherein anisotropically etching the isolation layer to form the body contact windows and the first contact window includes a two-step etching process which comprises:

removing portions of the isolation layer and the gate oxide layer by etching to form the body contact windows and the first contact window; and

removing an exposed portion of the polysilicon plate at the first contact window, and removing an exposed portion of the N+ diffused regions at the body contact windows.

11. The method of claim 1, wherein patterning and anisotropically etching to form the body contact windows and the first contact window comprises removing the isolation layer and the gate oxide layer by etching while using the polysilicon plate and the N+ diffused regions as etch stop layers.

12. The method of claim 1, wherein implanting P-type ions through the body contact windows to form the plurality of P+ diffused regions comprises providing a sufficient dose of the P-type ions to change an electric polarity of the N+ diffused region exposed by the body contact windows to the P+ diffused regions.

13. The method of claim 1, wherein the isolation layer comprises doped silicate glass.

14. The method of claim 1, wherein the source metal contact layer comprises a stack of Ti, TiN, and AlSiCu alloy layers.

15. A method of forming a trenched DMOS device and a termination structure thereof, the method comprising:

providing an N+ silicon substrate, an N- epitaxial layer on the N+ silicon substrate, a termination oxide layer on the N- epitaxial layer, a P body in the N- epitaxial layer, a plurality of DMOS trenches extending through the P body into the N-epitaxial layer, and a gate oxide layer over exposed surfaces of the P body;

forming a trenched DMOS device having a plurality of polysilicon gates disposed in the DMOS trenches, and a polysilicon plate disposed over the termination oxide layer and over a portion of the gate oxide layer disposed adjacent the termination oxide layer;

implanting N-type ions into a portion of the P body not covered by the polysilicon plate and termination oxide layer to form a plurality of N+ diffused regions;

forming an isolation layer over exposed surfaces after implanting the N-type ions;

patterning and etching the isolation layer and the gate oxide layer to form a plurality of body contact windows over the N+ diffused regions, and a first contact window over the polysilicon plate;

implanting P-type ions through the body contact windows to form a plurality of P+ diffused regions; and

forming a source metal contact layer over the isolation layer, and filling the body contact windows and the first contact window.

16. The method of claim 15, further comprising forming a drain metal contact layer on a back surface of the N+ silicon substrate.

17. The method of claim 15, wherein the polysiliccype ate comprises a portion extending toward one of the DMOS trenches disposed closest to the polysilicon plate.

23. A method of forming a trenched DMOS device and a termination structure thereof simultaneously, the method comprising:

providing a silicon substrate with an epitaxial layer formed thereon, and a body region defined by doping the epitaxial layer;

selectively etching the body region to form a plurality of DMOS trenches therein;

forming a gate oxide layer over exposed surfaces in the body region and a termination oxide layer to cover the body region;

depositing a polysilicon layer over exposed surfaces;

selectively etch the polysilicon layer to form a plurality of polysilicon gates in the DMOS trenches and a polysilicon plate having an extending portion toward the body region over the termination oxide layer;

forming sources in the body region by using the polysilicon plate as a mask; and

forming an isolation layer and then a source metal contact layer over exposed surfaces, the isolation layer protecting the polysilicon gates, the source metal contact layer grounding the body region and the polysilicon plate.